

## Scale-Up: From Monolithic Silicon to Advanced Packaging

October 15, 2026 | Chetan Arvind Patil, Marvell Technology

Estimated reading time: 3 minutes



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This is the first in a three-part series exploring scale-up, scale-out, and scale-across in advanced packaging. Scale-up focuses on increasing compute capability, memory capacity, and communication bandwidth within tightly integrated computing systems. Scale-out expands computing capacity by connecting multiple servers, compute nodes, and racks through high-speed networks. Scale-across focuses on integrating and coordinating diverse computing resources, technologies, and workloads across data centers to improve overall efficiency and resource utilization.

While these three approaches address different scaling requirements, advanced packaging plays a critical role in enabling each. This first article focuses on scale-up, tracing its evolution from monolithic silicon to package-level integration, the practical challenges it faces, and the technologies shaping its future.

### Evolution of Scale-Up From Monolithic Silicon to Advanced Packaging

For decades, semiconductor scale-up focused on increasing computing capability within a single silicon die. Manufacturing advances enabled smaller transistors, higher transistor density, more processing cores, and larger on-chip caches. This approach allowed semiconductor companies to continuously improve performance through monolithic silicon designs.

However, as chip designs grew larger and more complex, traditional scaling faced practical limits. Lithography reticle limits restricted the maximum die size, while larger dies increased manufacturing costs and yield risk. Higher transistor density also introduced challenges in power consumption, heat dissipation, and interconnect performance. These limitations encouraged semiconductor companies to explore alternatives to larger monolithic designs.

Advanced packaging introduced another approach to scale-up by enabling multiple silicon dies to operate within a common package. Instead of relying on a single large die, semiconductor companies could integrate smaller dies using HDIs. Technologies such as 2.5D integration, silicon interposers, embedded bridges, and 3D stacking enabled greater package-level computing capability. TSMC's CoWoS, Intel's EMIB, and Foveros are examples of technologies supporting this transition.

| Scaling Parameter   | Monolithic Silicon                                    | Scale-Up Advanced Packaging                                       |
|---------------------|-------------------------------------------------------|-------------------------------------------------------------------|
| Compute Integration | More transistors and cores within one die             | Multiple compute dies within one package                          |
| Physical Scaling    | Limited by die size and reticle constraints           | Extends integration beyond a single die                           |
| Memory              | On-chip cache and external memory                     | HBM integrated close to compute                                   |
| Interconnect        | Primarily on-die connections                          | High-density die-to-die connections                               |
| Manufacturing       | Larger dies increase yield risks                      | Smaller dies offer yield advantages, but assembly adds complexity |
| Packaging Role      | Primarily electrical, mechanical, and thermal support | Enables compute and memory integration                            |

Table 1: Scale-up has evolved from monolithic silicon to advanced packaging

The transition to advanced packaging does not replace traditional transistor scaling. Instead, it complements silicon technology improvements by enabling more computing and memory resources to be integrated into a tightly connected package. This matters especially for AI accelerators and high-performance computing, where increased compute capability must be supported by sufficient memory bandwidth and efficient communication.

Scale-up is therefore evolving from increasing a single silicon die's capability to increasing the combined compute, memory, and communication capability of an entire semiconductor package.



Figure 1: Scale-up in advanced semiconductor packaging brings multiple compute dies and high-bandwidth memory (HBM) into a single package, using high-density die-to-die interconnects to increase processing capacity, improve data transfer, and reduce latency.

### Practical Challenges Of Package-Level Scale-Up

Advanced packaging enables scale-up by increasing computing capability, memory bandwidth, and integration density within a single semiconductor package. However, integrating more compute dies, memory stacks, and interconnects introduces technical and manufacturing challenges affecting performance, reliability, and cost. One primary challenge is power delivery and thermal management. As scale-up architectures integrate more high-performance dies, power demand and heat generation rise. Efficient power distribution and cooling solutions become essential, especially for larger packages and vertically stacked dies.

Another challenge is die-to-die interconnect performance. Scale-up requires high-bandwidth, low-latency communication between compute dies and memory. More dies increase routing complexity, signal integrity concerns, and interconnect power consumption, making efficient communication critical to overall performance.

Manufacturing yield and cost also grow more important. Advanced packages with multiple compute dies and HBM stacks require precise assembly and bonding. Larger packages bring challenges in warpage, alignment, and reliability, and defects during integration can increase manufacturing losses. Testing adds complexity, making known-good die selection and package-level validation essential. Ultimately, successful scale-up depends on balancing compute performance, power

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dies within a package.

#### Next-Gen Scale-Up Through Advanced Packaging

The next generation of scale-up will focus on increasing computing capability, memory bandwidth, and integration density within advanced semiconductor packages. Growing demands for AI and HPC require more compute and memory resources while maintaining power efficiency and reliable operation.

One major direction is expanding 2.5D packaging, where larger interposers and advanced redistribution technologies enable more compute dies and HBM stacks in a single package. Meanwhile, 3D integration and hybrid bonding will support greater integration density through vertical stacking and finer die-to-die connections.

However, increasing package complexity requires improvements in power delivery, thermal management, manufacturing yield, and testing. Advanced substrates, efficient cooling solutions, and precise assembly processes are essential to support larger, denser packages. The future of scale-up depends not simply on integrating more silicon but on how efficiently compute, memory, and interconnects operate together. Advanced packaging remains central to balancing performance, power efficiency, reliability, and manufacturing costs.

Now that we've established scale-up as the first dimension of advanced packaging-driven semiconductor scaling, the next article will explore scale-out, focusing on expanding computing capacity by connecting multiple servers, compute nodes, and racks through high-speed networks, followed by scale-across, which examines the integration and coordination of diverse computing resources and workloads across data centers.

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##### CSP CapEx to Exceed US\$1.5T in 2027 as AI Server Revenue Surges

10/14/2026 | TrendForce

Hyperscale CSPs are ramping up investments in servers and AI infrastructure, according to TrendForce's latest AI server industry research.

##### Kapta Space Raises \$24M Series A, Secures Multiple Classified MTI Contracts

10/13/2026 | Kapta Space

Kapta Space, a developer of next-generation spaceborne radar payloads, today announced a \$24 million Series A financing led by Washington Harbour Partners and co-led by Bison Ventures, with participation from MetaVC and a group of new and existing investors including MYDA Capital, Entrada Ventures, Aurelia Foundry, and Fitz Gate Ventures.

##### CScale Exits Stealth With \$145M to Build AI Interconnects

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CScale exited stealth, announcing \$145 million in Series C funding to accelerate development and commercialization of optical interconnect for AI scale-up, the high-bandwidth, ultra-low-latency connections that let accelerators work together like a single, much larger computer.

##### Samsung Commits \$1 Billion to Helix Digital Infrastructure for AI Buildout

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