New Silicon Demands New Test Technologies

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The semiconductor industry has entered an era where packaging innovation is advancing just as rapidly as transistor technology. AI and high-performance computing (HPC) processors increasingly integrate compute chiplets, high-bandwidth memory (HBM) stacks, networking interfaces, analogue circuitry, security processors and specialised accelerators within a single package. These components are frequently fabricated using different process technologies before being assembled into highly integrated heterogeneous systems.

Such an architectural evolution introduces testing challenges that extend far beyond traditional manufacturing verification. A functional defect may originate within an individual die. At the same time, performance degradation could result from faulty die-to-die communication, package assembly defects, thermal interactions, or signal integrity issues across thousands of interconnects. In advanced packages, even minor imperfections in interposer connections, hybrid bonding interfaces, or through-silicon vias (TSVs) can significantly affect overall system performance.

Testing has therefore expanded beyond wafer probe and final package verification. Test engineers must now validate package assembly, high-speed communication links, embedded monitoring circuitry, power delivery networks, thermal behaviour and increasingly complex interactions between multiple heterogeneous devices. System validation often continues during board integration, server qualification, and even after deployment through continuous health monitoring and predictive diagnostics.

Meeting these requirements demands standardised methodologies that allow designers, manufacturing partners, test equipment suppliers and system integrators to access and evaluate increasingly sophisticated semiconductor devices using common architectures. This is where the test standards provide this common foundation, enabling consistent development of tools, methodologies and workflows across the global semiconductor ecosystem.

Test standards supporting modern semiconductor test

The rapid evolution of semiconductor technology has been accompanied by an equally significant transformation in semiconductor test methodologies. As devices have progressed from conventional integrated circuits to complex AI and HPC systems incorporating advanced packaging, chiplets and heterogeneous integration, new testing challenges have emerged across every stage of the product lifecycle. To address these challenges, industry test standards have evolved to provide common architectures, methodologies and interfaces that enable consistent, scalable and interoperable testing solutions.

Rather than serving as isolated specifications, these standards collectively establish the foundation for modern semiconductor test, supporting everything from board-level connectivity and automated test data exchange to embedded instrumentation, advanced package validation, chiplet integration and system-level diagnostics.

Together, these test standards illustrate the continuous evolution of semiconductor testing in response to changing device architectures and manufacturing technologies. While each standard addresses a specific aspect of test, their collective contribution extends far beyond individual applications. They enable a standardised ecosystem that supports interoperability between design tools, test equipment, manufacturing processes and system validation workflows. As AI and HPC devices continue to increase in complexity,

Test Technology Area	Representative Standards	Purpose
Test Access and Boundary Scan	1149.1, 1149.4, 1149.6, 1149.7, 1149.10.	Standardised access to devices, boards, mixed-signal circuits and high-speed interfaces.
Test Data and Automation	1450 family (1450, 1450.1, 1450.4, 1450.6.2).	Standardised representation of test vectors, test flows and design information.
Embedded Test and Instrumentation	1500, 1581, 1687 Family (1687, 1687.1, 1687.2).	Standardised access to embedded IP, sensors, monitors and on-chip instruments.
Quality and Coverage	1804, 2427.	Fault accounting, coverage reporting and analogue defect modelling.
Advanced Packaging and 3D Integration	1838, 1838a.	Test architectures for stacked dies, multi-die packages and advanced interconnects.
System-Level Test & Debug	2654, 2929.	System test access and functional state extraction.
Chiplet Test and Repair	3405.	Standardised die-to-die interconnect testing and repair.

Table 1: Test technology areas and their associated standards

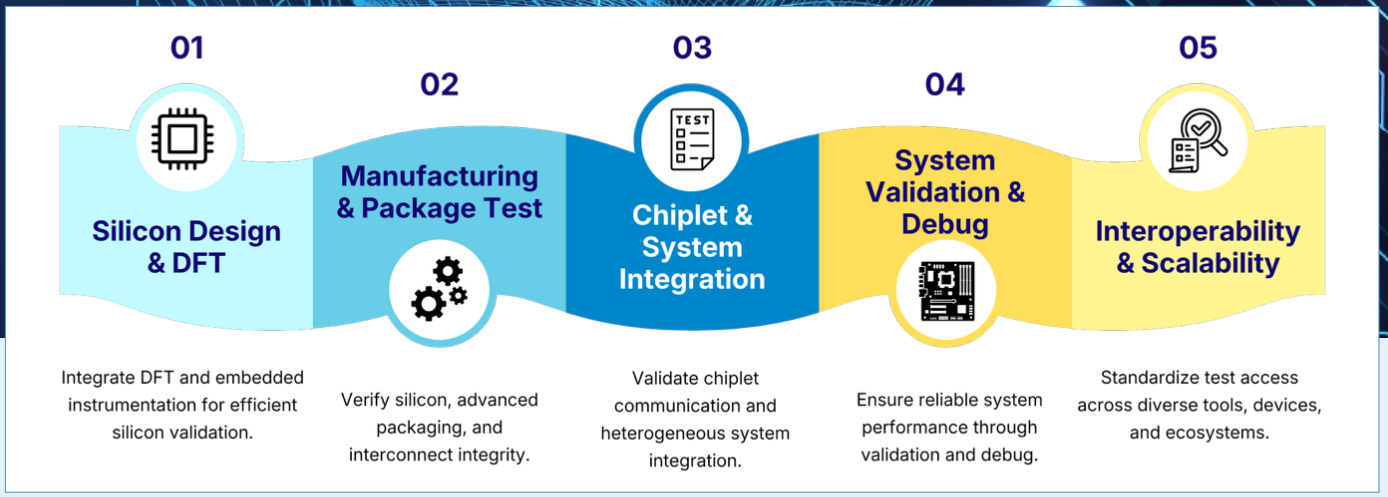

Figure 1: The next frontier of semiconductor testing

these standards will remain instrumental in driving innovation across semiconductor test technologies, ensuring that future generations of advanced silicon can be manufactured, validated and deployed with greater reliability, scalability and confidence.

Standards enabling the next generation of semiconductor test

One of the most significant contributions of modern test standards is the establishment of standardised test access architectures for increasingly complex semiconductor devices. As transistor counts have grown into the 10s of billions, dedicated test pins for every internal circuit have become impractical. Standardised interfaces provide efficient access to internal logic, embedded sensors, memory subsystems and debug resources through common infrastructures, simplifying manufacturing test, post-silicon validation and debug while enabling greater reuse of test methodologies across multiple device families.

The adoption of advanced packaging technologies has significantly expanded the scope of semiconductor testing. Technologies like 2.5D integration, 3D stacking, HBM, silicon bridges and hybrid bonding introduce thousands of high-density interconnects that require validation throughout manufacturing and assembly. Modern test standards provide architectures for testing stacked dies, advanced package interconnects and multi-die assemblies. As chiplet-based designs become mainstream, they also enable standardised approaches for die-to-die interconnect testing and repair, ensuring reliable communication across heterogeneous chiplets.

Testing has also evolved beyond manufacturing verification into continuous product validation. Modern AI processors incorporate embedded sensors that monitor temperature, voltage, current, timing margins and device health throughout operation. Standardised access to these embedded instruments supports silicon characterisation, board bring-up, system integration and in-field diagnostics, allowing test data to improve both manufacturing quality and long-term system reliability.

This evolution extends to the system level, where AI platforms integrate processors, accelerators, HBM, networking and storage into tightly coupled computing systems. Test standards supporting system-level access and state extraction enable coordinated validation across multiple devices while simplifying debug of increasingly complex software-hardware interactions. By providing common methodologies across foundries, outsourced semiconductor assembly and test (OSAT) operations, electronic design automation (EDA) vendors, equipment suppliers and system integrators, these standards improve interoperability, accelerate innovation and enhance manufacturing efficiency across the semiconductor ecosystem.

The pace of semiconductor innovation continues to accelerate as AI workloads demand higher computational density, greater memory bandwidth and improved energy efficiency. Future computing platforms will integrate larger chiplet ecosystems, co-packaged optics, silicon photonics, CXL-enabled memory expansion and increasingly intelligent power and thermal management technologies. These innovations will not only increase system complexity - but also introduce new validation challenges spanning silicon, advanced packaging, interconnects, firmware and complete system integration.

At the same time, testing is becoming more data-driven, with embedded telemetry, continuous health monitoring and predictive analytics enabling adaptive diagnostics that extend well beyond traditional manufacturing test. These capabilities will allow engineers to monitor device health throughout deployment, identify early signs of degradation and improve system availability in large-scale AI infrastructure.

As semiconductor architectures continue to evolve, test standards will remain fundamental to developing scalable, interoperable and reliable validation methodologies. By providing common frameworks for test access, embedded instrumentation, advanced packaging, chiplet integration, system-level validation and lifecycle monitoring, these standards enable the industry to address the growing complexity of AI and HPC silicon while fostering collaboration across the semiconductor ecosystem.

Looking ahead, emerging technologies and new system architectures will continue to drive the evolution of test standards, ensuring they remain aligned with future industry requirements. Testing is no longer the final manufacturing checkpoint - it has become an integral part of design, manufacturing, deployment and long-term operation, helping ensure the performance, reliability and scalability of next-generation computing platforms.