More Than Moore Enabled by Advanced Packaging and Heterogeneous Integration

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Advanced Packaging a Key Enabler for System Integration

For more than a half-century, Moore's Law has been the defining principle of semiconductor innovation. By continually shrinking transistor dimensions, the semiconductor industry delivered exponential improvements in computing performance, energy efficiency, and integration density. Each new technology node enabled more transistors to be placed on a single die, reducing the cost per transistor and making electronic systems smaller, faster, and more capable.

Though this scaling continues to advance, it is no longer the sole driver of system-level innovation, which now increasingly comes from a combination of scaling and advanced packaging. But as devices approach the practical limits of silicon scaling, the challenges associated with manufacturing complexity, power density, reticle size, yield mean a substantial rise in development costs. Building larger monolithic integrated circuits (ICs) has thus become both technically challenging and economically demanding.

For these reasons, rather than relying exclusively on transistor miniaturization, the semiconductor industry has now embraced a complementary approach known as "More than Moore," in which advanced packaging solutions play a more important role in the overall system equation. Instead of asking how many more transistors can fit on a chip, designers are focused on how multiple optimized semiconductor technologies can be integrated into a single package. This shift places advanced packaging and heterogeneous integration at the center of continued semiconductor scaling, transforming the package from a protective enclosure into an active enabler of system innovation.

Advanced Packaging: The New Engine of System Scaling and Operational Success

Historically, semiconductor packaging served a relatively straightforward purpose. Once fabricated, the silicon die was enclosed in a package that provided mechanical protection, electrical connections to the PCB, and heat dissipation. While packaging technologies steadily evolved to support higher pin counts and improved reliability, most system innovation occurred within the silicon itself.

That relationship has fundamentally changed over the past few years. Modern electronic systems demand significantly higher computational performance, greater memory bandwidth, improved power efficiency, and greater diverse functionality.

Achieving these requirements on a single monolithic die has become more difficult. Larger dies often experience lower manufacturing yield, increased design complexity, and higher production costs. At the same time, not every circuit within a system benefits equally from the most advanced process technology. Logic, memory, analog, RF, power management, and photonic devices often have distinct manufacturing requirements and optimal process nodes.

Advanced packaging addresses these challenges by allowing multiple semiconductor dies to function as a single, unified system within a single package. Instead of forcing every function onto a single large chip, designers can partition complex systems into smaller functional building blocks (chiplets), each optimized independently and interconnected through advanced packaging technologies.

This modular design philosophy provides advantages well beyond manufacturing efficiency:

- Individual chiplets can be reused across multiple product families
- Design updates can be implemented without redesigning an entire system
- Future technologies can be incorporated more rapidly through package-level integration

The result is a more flexible and scalable development model that supports faster innovation while reducing overall system complexity. System performance is determined not only by transistor density but also by how efficiently these individual components communicate with one another.

In many respects, the package has become a critical enabler for system miniaturization and performance.

From Monolithic Integration to Heterogeneous Systems

In traditional ICs, the attempt was to incorporate as many system functions as possible onto a single piece of silicon. While this approach simplified integration, it also imposed significant compromises. Every function had to share the same manufacturing process, regardless of whether that process was optimal for each individual circuit. As chip sizes increased, manufacturing yield decreased, development costs escalated, and product flexibility diminished.

Aspect	Monolithic Integration	Heterogeneous Integration
Architecture	Single large SoC	Multiple chiplets integrated within one package
Process Technology	Single process node for all functions	Different process nodes optimized for compute, memory, analog, RF, and I/O
Manufacturing Yield	Lower yield as die size increases	Higher yield with smaller, independently fabricated dies
Design Flexibility	Limited design reuse and scalability	Modular architecture enables reusable IP and faster product development
Performance Scaling	Primarily through transistor scaling	Through both transistor scaling and advanced package level integration
System Performance	Limited by monolithic die size and on-chip resources	Higher bandwidth, lower latency, and improved power efficiency through optimized interconnects
Scalability	Constrained by reticle size and die complexity	Easily scalable by adding or upgrading individual chiplets
Typical Applications	Consumer SoCs, MCUs, conventional processors	AI, HPC, networking, automotive, communications, and edge computing

Table 1: Diverging solutions to enduring challenges: How heterogeneous and monolithic architectures differ

Heterogeneous integration takes a fundamentally different approach. Individual functional blocks,

networking devices, and specialized accelerators, are manufactured separately using the process technology best suited to each function. These independently optimized dies are then assembled into a single package, where they operate as a unified, highly integrated system.

Packaging Technologies That Enable System Integration and Miniaturization

Advanced packaging technologies have made heterogeneous integration practical for a wide range of semiconductor applications. Conventional 2D packaging serves many products effectively, but more demanding applications now require substantially greater interconnect density and bandwidth.

This has driven the adoption of 2.5D integration, where multiple semiconductor dies are interconnected through a silicon interposer that provides thousands of high density signal connections. By shortening communication paths between devices, 2.5D integration enables significantly higher bandwidth and lower latency while reducing power consumption compared to traditional board-level interconnections. (Glass and organic interposers are not discussed in the scope of this article. I hope to address them in another.)

Three-dimensional integration extends this concept by stacking semiconductor dies vertically. Through-silicon vias (TSVs) and, more recently, direct hybrid bonding technologies create extremely short electrical pathways between stacked devices, enabling higher integration density, higher bandwidth, and improved energy efficiency. Vertical integration also reduces the physical footprint of complex systems while supporting faster communication between closely coupled functional blocks.

The industry is now extending these concepts even further through sophisticated multi-die architectures that combine multiple interposers, bridges, and stacked devices within a single package. Rather than viewing packaging as the final manufacturing step, semiconductor companies treat package architecture as a critical design decision that directly influences system performance, scalability, reliability, power efficiency, and manufacturing cost.

This continued evolution of advanced substrates, fine-pitch interconnects, high density redistribution layers, and precision assembly processes is expanding the possibilities for integrating diverse semiconductor technologies within a common platform.

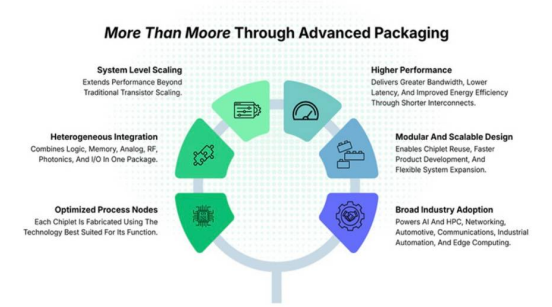

Figure 1: More Than Moore through advanced packaging.

System-level Scaling Enabled Through Advanced Packaging

This system-level integration approach enables designers to combine compute, memory, analog, RF, photonics, and power management devices using the process technology best suited for each function. The result is higher performance, greater memory bandwidth, lower latency, improved energy efficiency, and enhanced design flexibility without relying solely on larger monolithic chips.

AI and HPC platforms leverage chiplets and high-bandwidth memory to accelerate data-intensive workloads. Networking and telecommunications equipment integrate high-speed processors, switching silicon, and optical interfaces to meet growing bandwidth demands. Automotive systems combine processors, sensors, memory, and power devices to support ADAS, autonomous driving, and vehicle electrification. Similar heterogeneous architectures are also emerging in industrial automation, aerospace, medical electronics, and edge computing, where performance, reliability, and power efficiency are equally critical.

More than Moore complements Moore's Law by extending innovation through heterogeneous integration and advanced packaging, rather than relying solely on transistor scaling.

As electronic systems become more complex and application-specific, advanced packaging and heterogeneous integration, driven by More Than Moore methodology, will provide the flexibility and scalability needed to integrate diverse technologies into highly integrated, compact, and high performance systems.

The package is, thus, no longer simply the final step in manufacturing. It has become a key enabler of the next generation of semiconductor-driven computing innovation, supporting modular architectures, heterogeneous integration, and application-optimized system design. As demands increase across AI, HPC, networking, automotive, communications, industrial electronics, and edge computing, advanced packaging will play a central role in delivering the performance, scalability, and energy efficiency required by future electronic systems.

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Raytheon, an RTX business, and Composite Energy Technologies (CET) have successfully demonstrated the undersea launch capabilities of HADALUS, a new, low-cost, long-endurance unmanned undersea vehicle (UUV).

LITEON Invests in DenseLight to Strengthen Optical Communications for AI Infrastructure

08/04/2026 | LITEON Technology

LITEON Technology announced a strategic investment in DenseLight Photonics, a provider of indium phosphide (InP) optical communication components through its Singapore-based operating subsidiary, with a total transaction value of US$34.3 million.

Cicor Reports Strong H1 Orders, Returns to Organic Growth in Q2

07/22/2026 | Cicor

Cicor Group achieved strong growth in revenue and orders in the first half, while profitability and cash conversion reflected the ongoing integration phase and supply chain challenges.

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