System Architecture Beyond the Die With Advanced Packaging as the Scaling Factor

May 14, 2026 | Chetan Arvind Patil, Marvell Technology

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In conventional monolithic semiconductor design, system integration was achieved within a single die and constrained by reticle limits. Compute cores, cache, memory controllers, and input output (I/O) interfaces were all co-optimized on a single process node, with performance closely tied to transistor density and on-die interconnect efficiency. This monolithic system-on-chip (SoC) approach enabled low-latency communication and relatively straightforward power delivery. However, as design for compute-intensive SoCs approaches reticle limits and advanced-node costs increase, the ability to continue scaling within a single die begins to diminish.

At leading-edge advanced nodes (7 nm and below), these challenges become structural. Yield loss increases with die area due to higher defect density, while mask costs and process complexity continue to rise. At the same time, different functions do not scale uniformly. High-performance logic benefits from advanced nodes, while analog, I/O, and certain memory functions are more efficiently implemented on mature processes. Integrating all functions on a single die introduces inefficiencies in both cost and manufacturing utilization.

This imbalance is driving a shift in system construction. Instead of aggregating all functionality into a single die, advanced packaging enables integration at the package level. Multiple smaller dies, or chiplets, are combined within a single package, each fabricated on a process node best suited to its function. This improves yield, reduces cost exposure to advanced nodes, and introduces flexibility through reuse and modular design.

As integration moves beyond the die, complexity shifts toward assembly. Processes such as flip-chip die attach, micro-bump interconnect formation, and high-density substrate routing become central to enabling high-bandwidth communication between chiplets. Technologies such as silicon interposers, embedded bridges, and advanced organic substrates extend the interconnect fabric beyond the die, allowing multiple components to function as a unified system.

With this shift, considerations that were once secondary become critical. Package assembly must manage alignment accuracy, interconnect reliability at fine pitch, and consistent thermal behavior across heterogeneous dies. Test strategies also evolve, combining known-good-die validation before assembly with system-level testing after integration. Yield is no longer defined solely at the die level but across the entire assembly flow.

What emerges is a different model of integration. System functionality is no longer completed at tape-out but realized through assembly and validation at the package level. This naturally leads to a key question: Once integration moves beyond the die, how do packaging approaches begin to shape system architecture itself?

Packaging Technologies Defining System Integration

Once integration shifts to the package, the choice of packaging technology becomes central to system design. It is no longer only about connecting dies, but about determining how effectively they communicate, scale, and operate as a unified system.

As an example, 2.5D/3D integration using silicon interposers has become a foundational approach for high-performance systems. Platforms such as TSMC chip-on-wafer-on-substrate (CoWoS) enable large-scale integration of logic and high bandwidth memory (HBM) through fine-pitch routing across a silicon interposer. This allows very high interconnect density, supporting thousands of parallel connections between compute dies and memory stacks. While widely adopted in artificial intelligence (AI) accelerators, this approach introduces trade-offs in cost, package size, and manufacturing complexity.

To address these constraints, more localized integration techniques have emerged. Intel Embedded Multi-die Interconnect Bridge (EMIB) integrates silicon bridges within an organic substrate to enable high-density die-to-die connectivity without a full interposer. This reduces cost and improves scalability while preserving high-bandwidth links in targeted regions. In parallel, advances in organic substrates and redistribution layer scaling continue to improve routing density with better manufacturability.

Fan-out packaging further extends flexibility by redistributing input/output connections through multiple routing layers built directly on the package. Providers such as ASE and Amkor Technology have advanced wafer-level and even panel-level fan-out approaches to support multi-die integration at lower cost points. These solutions offer greater freedom in die placement and are increasingly being evaluated for systems requiring moderate interconnect density. At the same time, platforms such as Samsung Electronics I-Cube and H-Cube reflect a broader trend toward offering multiple integration options across performance and cost points.

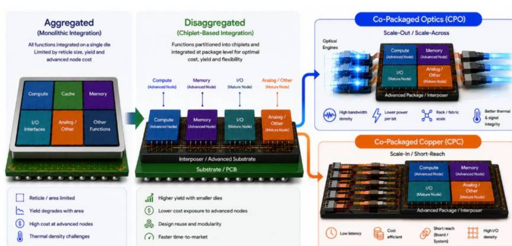

Figure 1: Advanced packaging extends system scaling beyond the die through disaggregated integration, enabling scale-in, scale-out, and scale-across architectures beyond traditional node-level limits. (Generated using GPT Image 2.0)

Alongside these approaches, efforts such as the Universal Chiplet Interconnect Express (UCIe) Consortium are introducing standardization, enabling interoperability across chiplets and supporting a more modular design ecosystem. As these technologies evolve, it becomes clear that packaging

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manufacturability constraints shape how chiplets are placed and connected. This naturally extends to how memory is integrated, where proximity, bandwidth, and placement begin to define system performance rather than simply support it.

Memory Integration and Package-Centric Architectures

As advanced packaging technologies define how chiplets are interconnected, they also shape how memory is integrated into the system. In high-performance and artificial intelligence (AI) systems, memory bandwidth has become a primary limiter, making data movement as critical as compute capability. This shifts memory from a peripheral element to a core part of system architecture, requiring tight integration within the package.

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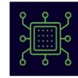

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HBM enables this by stacking dynamic random-access memory (DRAM) dies and connecting them through wide parallel interfaces. Advanced packaging allows these stacks to be placed close to compute dies, enabling high-density interconnects (UHDI) and improved data throughput. As a result, memory placement, stack count, and bandwidth distribution become key architectural decisions that directly influence package size, routing complexity, and system efficiency.

Design Factor	Packaging Impact	System Implication
Memory Stack Count	Increased routing density and assembly complexity	Higher bandwidth but larger package size
Memory Placement	Proximity to compute dies	Reduced latency and improved throughput
Bandwidth Distribution	Interconnect topology and routing layers	Balanced or bottlenecked system performance

Such a tighter integration introduces new constraints. Additional memory stacks increase substrate complexity and affect yield, while thermal interaction and shared power delivery must be carefully managed. As a result, system design becomes increasingly package-centric, reinforcing the shift toward disaggregated architectures where partitioning is closely tied to memory integration.

Scaling Disaggregated Design Further Through Co-Packaged Optics And Co-Packaged Copper

As advanced packaging pushes integration beyond the monolithic die, system bottlenecks are also shifting from compute density to data movement. This affects accelerators, switches, and rack-scale infrastructure. As a result, disaggregation is extending beyond the package, driving demand for high-bandwidth, energy-efficient interconnect architectures. In this context, co-packaged optics (CPO) and co-packaged copper (CPC) are critical technologies for next-generation scale-in, scale-out, and scale-across systems.

In scale-in architectures, advanced packaging technologies like silicon interposers, embedded bridges, and high bandwidth memory (HBM) enable dense local communication between compute chiplets and memory stacks. Yet, as artificial intelligence (AI) workloads distribute computation across several accelerators and nodes, interconnect scaling shifts from a package-level to a system-level challenge.

CPO addresses this challenge by integrating optical engines directly alongside switches or accelerator packages. This reduces the electrical trace length between the compute and the optical conversion. As a result, it significantly improves bandwidth density and lowers the power consumption associated with long-reach electrical signaling. Networking speeds are moving toward 800G, 1.6T, and beyond. CPO is becoming increasingly important for scale-out architectures, where traditional pluggable optics face limitations in signal integrity, front-panel density, and energy efficiency.

At the same time, CPC continues to play a critical role in short-reach, low-latency communication within servers and tightly coupled systems. CPC enables high-density electrical connectivity with lower manufacturing complexity and greater cost efficiency than optical integration. These technologies are not competing. Instead, CPC and CPO are evolving as complementary interconnect approaches. Copper remains optimized for localized communication within packages and boards. Meanwhile, optics increasingly enables scalable communication across racks and distributed compute fabrics.

The evolution of CPC and CPO extends advanced packaging from compute and memory integration into a broad networking infrastructure. The package thus becomes the launch point for system-level interconnects enabling large-scale, disaggregated computing.

Manufacturing Decisions for Disaggregation and Beyond

Lastly, as systems become more package-centric, partitioning moves to the forefront. Disaggregating functionality across chiplets is no longer only a design choice but a manufacturing strategy that directly impacts yield, cost, and scalability for silicon architecture designed for advanced computing like data centers. Instead of integrating everything on a single die, systems are now assembled from multiple optimized components within a package.

In monolithic designs, yield is constrained by die area, with larger dies more susceptible to defects. Partitioning into smaller chiplets improves yield and enables known good die strategies, where only validated components are integrated. It also allows different functions to be fabricated on process nodes best suited to their requirements, improving wafer utilization and reducing dependence on leading-edge nodes.

These benefits, however, shift complexity to the package. Assembly demands precise die placement, fine-pitch interconnect formation, and validation across multiple interfaces. Final yield depends not only on die quality but also on assembly precision and interconnect reliability, requiring test strategies that extend from wafer-level validation to full system-level verification.

This drives the partitioning decisions, which now sit at the intersection of design, packaging, and manufacturing. Advanced packaging specifically leads and defines how far disaggregation can scale and, in doing so, reshapes system architecture itself. The system is no longer defined by the limits of a single die, but by how effectively multiple dies can be integrated within the package. This shift certainly shows that the package has become the new scaling factor.

Chetan Arvind Patil is principal engineer, test engineering and customer strategy, at Marvell Technology.

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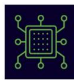

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