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Test & Yield Challenges of Chiplet-Based Semiconductor Products

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The semiconductor industry is fundamentally shifting how silicon (Si) chips are designed/manufactured. For decades, the primary approach when looking to increase performance and functionality was through the advancement of monolithic (aggregated) chip designs, where all the component elements were integrated into a single die. However, as the semiconductor industry approaches the limits of traditional scaling, due to economic/physical constraints, a new paradigm has now emerged - the chiplet.

At its core, a chiplet is a smaller, modular die that serves as a building block for creating complex systems. Instead of fabricating a single, massive chip, manufacturers can assemble multiple chiplets, with

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each of them being optimised for specific tasks. These can then be assembled into a single package.

Through this approach, greater design flexibility is enabled, with chip developers able to mix-and-match process nodes - using advanced nodes for performance-critical components and older nodes for cost-effectiveness. However, this modularity brings its own set of issues.

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