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# A cost analysis of the chiplet as a SoC solution

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The chiplet has become one of the most promising more-than-Moore (MtM) solutions, mainly for the system-on-a-chip (SoC) because it is nearing the reticle limit with every new process technology node. The SoC is also the ideal candidate for the chiplet, largely due to the ability to split the SoC's circuit blocks into multiple design and manufacturing flows, which can then be aggregated using advanced, heterogeneous integration solutions. Moreover, the SoC will eventually enable better power, performance, area, cost and time-to-market to be achieved.

AMD's EPYC and Ryzen processor families have already shown how impactful the chiplet is, for example, ways artificial intelligence (AI) workloads can make the most of new architectures developed with the chiplet. Slowly, the chiplet is also becoming the method of choice of emerging SoC startups such as

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Tenstorrent, which create chiplet-based architectures for the complex workloads that the computing industry will have to handle due to AI growth.

While no one can argue the benefits of incorporating a disaggregated way of using the chiplet to develop SoCs, one needs to take a close look at the cost impact on semiconductor manufacturing. It is, of course, crucial in making or breaking any silicon product and the basis of enabling a viable business for the vendors developing SoCs.

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