The Shift-Left Paradigm

Chetan Arvind Patil
Contributing Writer | EPDT

The semiconductor industry has historically grappled with high costs and delays, often caused by defects which have been detected late in production cycles. Studies have shown that defect resolution costs increase by up to 100x when identified in later stages compared to early detection during design. At the same time, the traditional approach to testing, which emphasises validation towards the end of development, frequently results in expensive and time-consuming rework.

Consider a groundbreaking approach that could transform the semiconductor industry - slashing costs, speeding up time-to-market and nurturing a more collaborative and efficient development environment. This is the potential of shift-left testing, which places early and continuous testing at the forefront throughout the semiconductor lifecycle.

Shift-left testing moves critical activities, such as design for testability (DFT), automated testing and predictive analytics, to the initial stages of the development process. By integrating these techniques early, the semiconductor product development team can identify and resolve defects on time, thereby significantly enhancing yield, reducing development costs and accelerating time-to-market.

This proactive methodology mitigates the risks associated with late-stage defect detection and fosters a more collaborative and efficient semiconductor product development environment.

Building for testability and yield

A successful shift-left strategy in semiconductor development hinges on 2 core factors - these are test and yield.

- Shift-left from a yield perspective - Optimising for yield necessitates the application of design for manufacturability (DFM) techniques, predictive yield modelling and process-aware design adjustments to maximise the production of functional devices. Early integration of these principles within the electronic design automation (EDA) workflow can substantially improve production efficiency. Utilising predictive analytics and machine learning to analyse historical production data helps identify patterns and potential yield issues. Real-time monitoring systems and feedback loops enhance yield optimisation by providing continuously updated insights into the production process, keeping semiconductor professionals in tune with their work. By focusing on these strategies, semiconductor companies can maximise yield, reduce production costs and consistently deliver high-quality products.

Yield Based Shift-Left Approach	Description
Predictive analytics and machine learning	Analyse historical production and yield data to identify patterns and predict potential yield issues.
Simulation and modelling	Use advanced simulation tools to predict yield issues and optimise designs before physical production.
DFM	Implement design rules and checks early to ensure manufacturability.
Prototyping	Rapid prototyping and iterative testing to refine designs and address yield issues early.
Advanced process control (APC)	Use statistical process control charts and adaptive control systems to maintain optimal production conditions.

Table 1: Key aspects of a yield-based shift-left approach

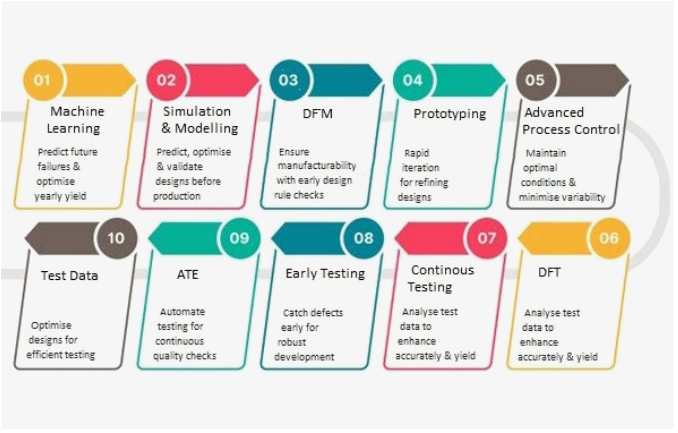

Figure 1: The elements involved in shift-left strategic implementations

- Shift-left from a test perspective - The role of technology in ensuring efficient testing is crucial. Building for testability involves integrating DFT principles, such as built-in self-test (BIST), boundary scan and scan chain insertion, to facilitate thorough and efficient testing from the earliest design stages. Early DFT integration ensures that testing considerations are embedded within the design process. Leveraging advanced simulation tools, such as SPICE for circuit simulation and Monte Carlo methods for statistical analysis, enables designers to predict and then mitigate potential testability issues.

Long-term benefits of shift-left

The long-term benefits of shift-left testing are increasingly critical as semiconductor technology advances to more complex nodes (such as 5nm, 3nm and beyond). Companies can improve product quality and reliability by testing earlier in the development cycle.

Test-Based Shift-Left Approach	Description
DFT	Integrate DFT principles, such as BIST and boundary scan, for easier and more efficient testing.
Continuous integration and continuous testing (CI/CT)	Develop automated testing pipelines and perform incremental builds to ensure continuous testing during development.
Early and incremental testing	Conduct unit tests, integration tests and system tests early and throughout the development process to catch defects sooner.
Automated test equipment (ATE)	Utilise ATE for high-coverage functional and parametric testing of semiconductor devices, plus implement parallel testing techniques.
Test data management and analytics	Collect detailed test data for performing failure examination to identify root causes, plus use test coverage analysis to identify testing gaps.

Table 2: Key aspects of a test-based shift-left approach

Detecting and resolving defects during the design phase can reduce defect-related costs by up to 80% compared to post-production fixes. This proactive approach is essential for advanced nodes, where even minor defects (such as a slight variation in transistor gate length) can reduce performance or cause yield losses.

Shift-left testing also significantly speeds up time-to-market by streamlining development processes and enabling iterative improvements. As companies transition to smaller nodes, rapid prototyping and validation becomes even more paramount. By detecting and addressing issues sooner, shift-left testing minimises costly rework, optimises resource allocation and enables more efficient new product introduction activity.

Furthermore, in advanced nodes, the integration of shift-left testing facilitates a more comprehensive analysis of the entire system-on-chip (SoC) architecture, accounting for interactions between various blocks and the interconnect fabric. By incorporating these considerations towards the beginning of the design process, shift-left testing helps to mitigate the risks associated with timing closure, power integrity and signal crosstalk, leading to more robust and reliable semiconductor devices.

Future trends in shift-left for semiconductor product validation

As the chip industry progresses towards ultra-advanced nodes (2nm and lower), the shift-left testing paradigm is going to be pivotal in enhancing product quality, yield and development efficiency. Companies can stay ahead of the curve by embracing early and continuous testing throughout development lifecycles.

The next generation of shift-left testing in semiconductor development will also be shaped by emerging innovations, including integration of artificial intelligence (AI) and machine learning (ML), transforming design-stage analysis and early defect detection, leading to improved design integrity and reduced late-stage fixes. Adopting these approaches will strengthen development processes and help maintain a competitive edge in the fast-changing semiconductor landscape.