Tracking Trillions of Parts Using Semiconductor ULT

In 2023, the global semiconductor industry shipped a total that was close to 1.2 trillion devices. Each of these devices went through a specific fabrication process, followed by assembly, testing and packing. In between these steps, they would have interacted with several workflows and various items of equipment. A process called unit-level traceability (ULT) is used to track all of these semiconductor production activities. In the following article, ***EPDT Contributor Chetan Arvind Patil*** *looks at what this involves and how this will be important with regard to greater manufacturer accountability, as well as combatting the rising prevalence of counterfeits.*

ULT is much more than identifying which fab or outsourced semiconductor assembly and test (OSAT) facility the parts came from. On top of this, it is also enabling troubleshooting via having a traceability flow that provides comprehensive detail about every interaction the device ever had with different pieces of equipment and process steps. Consequently, if a customer incident or field failure occurs, it is easier to trace things back - a crucial aspect of root cause analysis.

As such, semiconductor traceability systems can capture and record a wealth of data at every point of the manufacturing process. This ensures that each unit's history is documented from silicon wafer to finished product. Furthermore, ULT has clear value from the perspective of preventing counterfeit products entering the supply chain - with OEMs having greater visibility of where the devices they are incorporating into their equipment have come from and confidence with regard to the quality and functional capabilities of these devices.

Initial aspects of back traceability

One of the key steps in identifying precisely where a semiconductor device came from is capturing details that can connect it to the fab, OSAT or lot - and thus extrapolate that back to the exact wafer where it originated.

The genesis of this starts during testing or assembly, with the following approaches needing to be considered:

- Test-based ULT - Normally relying on the use of automated test equipment (ATE), test-based ULT is applied to devices with memories. During the wafer testing or final testing stages, the bits in the memory are flashed with codes to identify fab, OSAT, lot ID, wafer ID, die X and die Y. In the end, having lot, wafer and die X/Y data is itself more than enough, but if there are enough memory bits for ULT purposes, then including fab and OSAT (or internal assembly/test site) will further help during any subsequent failure analysis. Test-based ULT may also be referred to as electronic chip ID (ECID). One of the drawbacks associated with it is that if the memory is in some way damaged or corrupted, the ability to trace will be hindered. Also, as die sizes are shrinking (and thus package sizes too), incorporating sufficient memory blocks for this purpose is becoming more difficult - with them thus proving to be error-prone and not adequately robust. If test-based ULT doesn't work or won't fit due to lack of memory, then assembly-based ULT needs to come into the picture instead.
- Assembly-based ULT - Assembly-based ULT is the most widely used method of achieving device traceability. A device may or may not have memory, based on the design and budget requirements. However, as long as the front or the backside of the packaging process has enough space, traceability details can be laser-marked. Like ECIDs, assembly-based ULT also needs to improve on

the problem of errors where, during the failure analysis or handling of devices, the laser marking can become unreadable. However, as the semiconductor industry has advanced, the process has become less affected by errors, with marking/engraving now being more sophisticated. Eventually, it will be possible for all information to be laser-marked, depending on the package size.

These 2 approaches are specific to ULT. The semiconductor industry also relies heavily on other more generic tracking methods - such as barcodes to trace back the devices, wafers, lots, etc. However, those do not fall under unit-level processes.

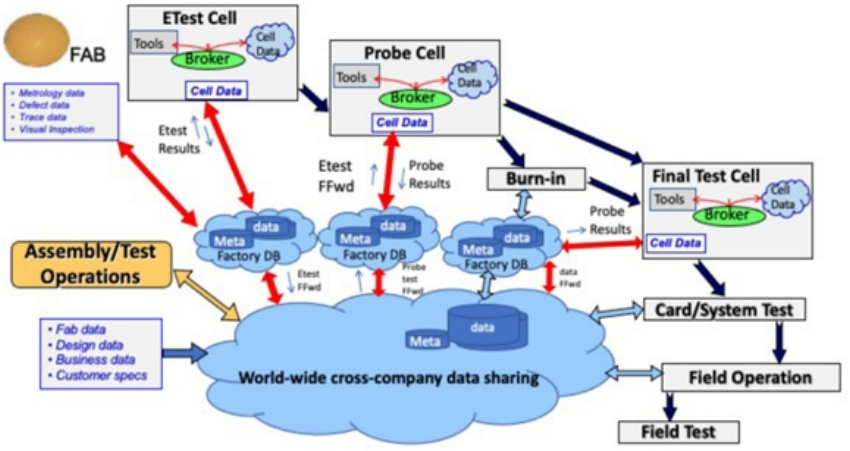

Figure 1: An adaptive test architecture - where each insertions test data is added to 1 or more databases so that it can be queried [Image source: IEEE]

The traceability data that ULT unlocks

The 1st step of finding a specific semiconductor unit's origins is to capture the lot, wafer and die X/Y details using either test or assembly-based ULT, per the device process flow. Having this information allows the following traceability data to be accessed:

- The fab that fabricated this device.
- The OSAT site that assembled and also carried out testing of this device (this could potentially be an internal facility of the semiconductor manufacturer itself too).
- The specific lot and wafer that the unit was assembled from.

When the above information is available, then it further facilitates matters in relation to the following data points for a specific unit:

- Which specific test program version was used during testing.
- Test, assembly and inspection data relating to the failed unit.
- The specific materials and assembly equipment that have been used during assembly and packaging.
- How the wafer was stored before it was tested/assembled.
- The exact ATE equipment used to test the unit and information on any potential issues with it.
- The fabrication process data for this unit.
- The nature of any test or assembly issue, based on the data on which the unit went through these process steps.
- •Any halting or downtime occurrence of the fab equipment during the fabrication of a failed unit - so that it can be determined if this contributed to the failure.
- How the data of the failed unit correlates to those that failed and originated from the same fabrication/assembly/testing flows.
- The ascertaining as to whether there were any wafer logistical/handling and storage errors.
- A possible similarity with any past failing history.

In summary, with just a few data points, ULT enables semiconductor companies to access an invaluable array of data points. These can help answer various different questions that will contribute to effective root cause analysis when the failure of a unit occurs.

Current process, gap and future of traceability

Traceability is already an essential part of manufacturing execution system (MES) implementations. Every fab, OSAT and even integrated device manufacturer (IDM) or fabless vendor producing semiconductor devices has its own dedicated MES which integrates with the production flow and captures the data points that can enable historical traceability information to be derived.

Such MES implementations will be capable of capturing data points at respective stages. They will then allow semiconductor engineers to learn about specific data excursions (from the standard process parameters/specs) that could have contributed to issues in the failing units. Recognised as a significant gap in today's MES strategy is that these implementations often work in isolation - meaning a fab will have its own proprietary MES, while an OSAT will have a completely different one, as will IDMs and fabless firms. Disconnected and distributed MES implementations with no interoperability between them will hinder the tracing of historical data, making the process more complex and time consuming.

As the semiconductor industry moves towards shipping even greater numbers of devices, there will be a need to further future-proof traceability processes - so that the time taken to capture the necessary historical data can be conducted faster. By leveraging some the connected solutions now emerging, it will be possible to create a free flow of information between all the different manufacturing process steps. Guidance on this is part of IEEE's Heterogenous Integration Roadmap.

Even using the existing infrastructure, semiconductor design and manufacturing houses are already able to trace huge quantities of data points. The only enhancement needed is with regard to the speed of data retrieval. The possibility of employing artificial Intelligence (AI) to summarise all the information as soon as lot, wafer and die X/Y details are shared is certainly something that needs investigation.