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A cost analysis of the chiplet as a SoC solution

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The chiplet has become one of the most promising more-than-Moore (MtM) solutions, mainly for the system-on-a-chip (SoC) because it is nearing the reticle limit with every new process technology node. The SoC is also the ideal candidate for the chiplet, largely due to the ability to split the SoC's circuit blocks into multiple design and manufacturing flows, which can then be aggregated using advanced, heterogenous integration solutions. Moreover, the SoC will eventually enable better power, performance, area, cost and time-to-market to be achieved.

AMD's EPYC and Ryzen processor families have already shown how impactful the chiplet is, for example, ways artificial intelligence (AI) workloads can make the most of new architectures developed with the chiplet. Slowly, the chiplet is also becoming the method of choice of emerging SoC startups such as Tenstorrent, which create chiplet-based architectures for the complex workloads that the computing industry will have to handle due to AI growth.

While no one can argue the benefits of incorporating a disaggregated way of using the chiplet to develop SoCs, one needs to take a close look at the cost impact on semiconductor manufacturing. It is, of course, crucial in making or breaking any silicon product and the basis of enabling a viable business for the vendors developing SoCs.

A cost comparison of aggregated and disaggregated SoC development methods

Cost of aggregated SoC development—the non-chiplet way

Aggregated SoC development features one specific advanced technology node and involves one dedicated manufacturing flow that takes SoC design to fabrication, through to assembly, testing and packing. The cost

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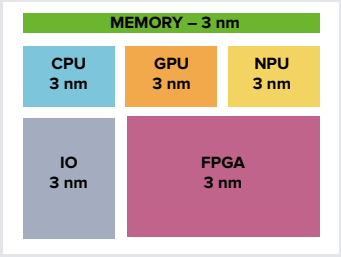
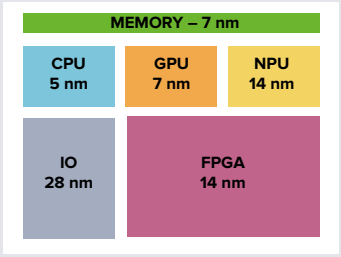
Non-Chiplet SoC



Aggregated fabrication with all the blocks using one specific technology node

Chiplet SoC



Disaggregated fabrication with blocks using different technology nodes

is down to a mix of the workers required to design and manage manufacture the SoC die and the manufacturing flow itself.

Aggregated SoC development costs can be summarised as technology node, testing time, yield, assembly cost, test cost and miscellaneous cost adders. A single manufacturing flow is a positive, since it requires fewer resources (equipment, manpower, etc.). That said, the advanced technology nodes increase the field-effective transistor (FET) counts and can lead to lower yields and higher test times. In addition, an advanced and therefore more costly technology node may not be required for all SoC dies.

Lastly, there is no need to re-validate the dies for their intended application. If a die passes the test stage, it is deemed good for application.

Non-chiplet cost model

Single manufacturing flow:

technology node cost + testing time + yield + assembly cost + test cost + miscellaneous cost adders.

Technology node includes mask and wafer costs.

Cost of disaggregated SoC development—the chiplet way

Disaggregated SoC development involves taking a set number of the SoC's FETs and splitting them into groups, using multiple manufacturing flows to produce these groups as chiplets or silicon blocks and then assembling these into the SoC. The technology nodes used are a mix of advanced (some blocks requiring the same node as non-aggregated SoC) and matured (some blocks requiring an older node).

The multiple flows increase cost not only in terms of their setting up and running but their requiring multiple teams to design and manufacture the various chiplets. Further increasing the cost are the factors of advanced packaging (heterogeneous integration) and application test and yield or re-validation. Advanced packaging is the assembly of the chiplets from the different manufacturing flows into the SoC dies. Application test and yield is the revalidation of the chiplets for their intended application to ensure they and the SoC dies are working. So, disaggregated SoC development costs for each flow are technology node, testing time, yield, assembly cost, test cost, miscellaneous cost adders, advanced packaging (heterogeneous integration) cost and application and yield cost.

In summary, the chiplet way of SoC development is technologically beneficial. However, it is not a given that the business case applies to all SoC design and manufacturing. It is a trade-off that SoC vendors would have to review thoroughly.

Way forward

Chiplet cost model

Multiple manufacturing flows:

No. of chiplets x (technology node cost + testing time + yield + assembly cost + test cost) + advanced packaging (heterogeneous integration) cost + miscellaneous cost adders + application test and yield cost

Technology node includes mask and wafer costs.

Today, the chiplet is the most viable way for SoC vendors to utilise the most advanced and mature nodes. With Intel, Samsung and TSMC marching towards 2 nm nodes, the chiplet will be crucial in enabling central processor unit (CPU) and graphics processor unit (GPU) design and incorporating specialised processing elements (PEs) to speed up AI frameworks and models.

One potential way to mitigate the added cost of the chiplet is to thoroughly review which groups to disaggregate and which to keep tied together. This should be done at the intellectual property (IP) level so that SoC vendors can repeat the new revisions faster, which would be crucial when they start utilising ultra-advanced, 3 nm and smaller nodes.

To conclude, the chiplet has tremendous potential to revolutionise SoC and other complex silicon development. However, SoC vendors must develop cost strategies to make it viable. ■

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