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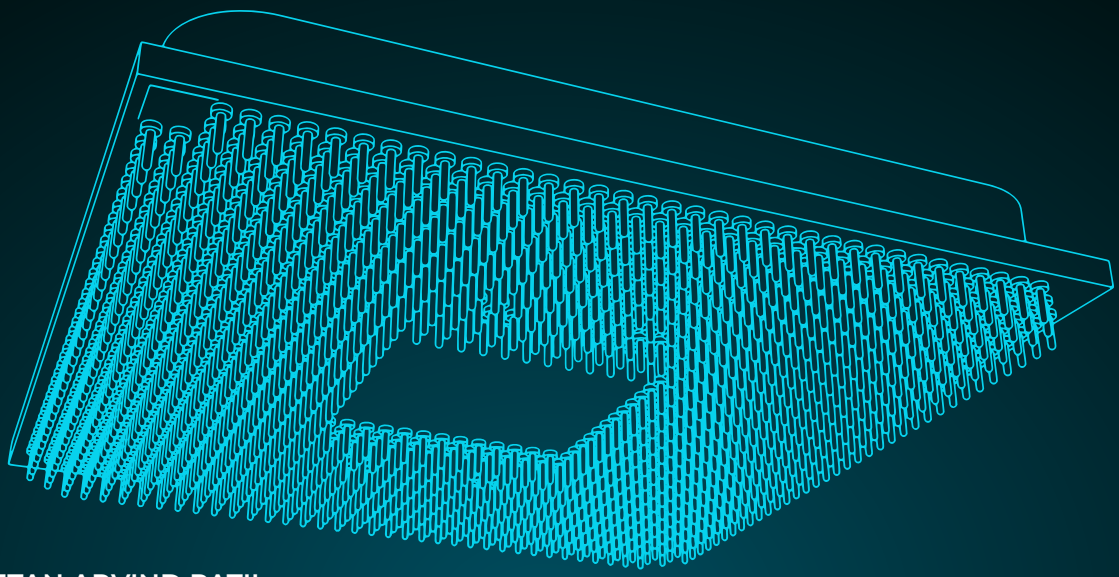
Single chiplet type versus multiple chiplet types per wafer methods



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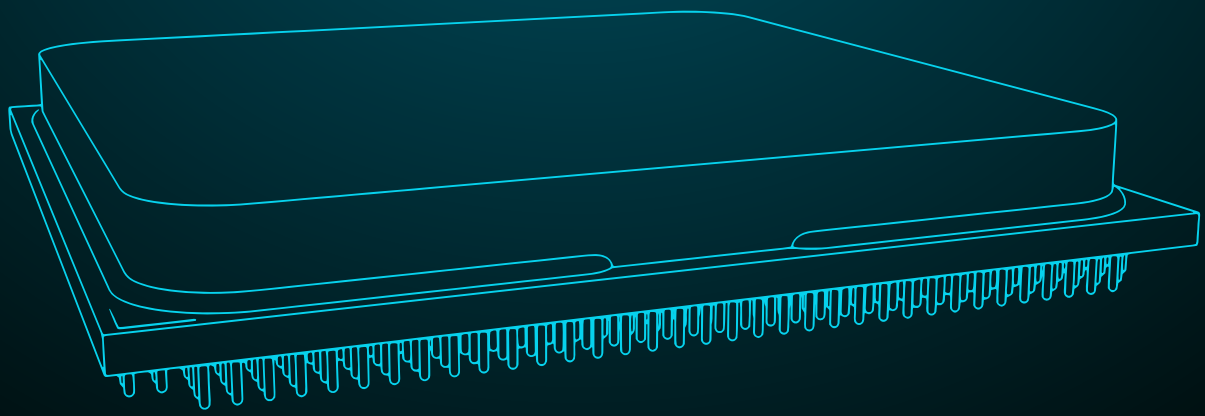
As discussed in the previous issue, the term 'chiplet' has gained prominence in semiconductor design and manufacturing as a solution to some of the challenges presented by Moore's Law slowing down. Instead of integrating all functions on a monolithic die, the chiplet method disaggregates the monolithic die into smaller, modular dies or chiplets that can be manufactured separately and assembled on an interposer or package.



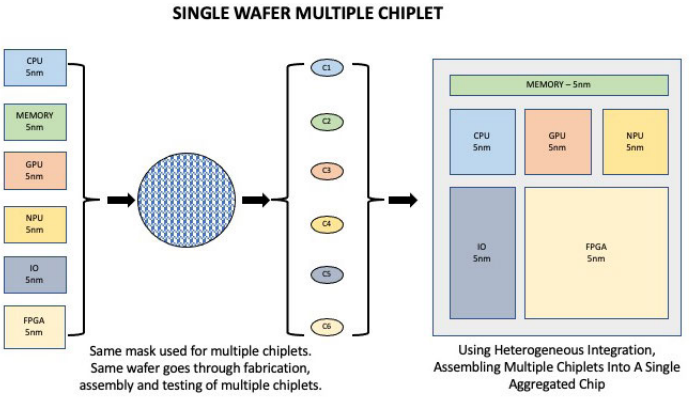
There are two ways in which chiplets can be manufactured: single chiplet type per wafer or multiple chiplet types per wafer.

Single chiplet type per wafer method

In the single chiplet type per wafer method, a wafer will carry one chiplet type. This means that every chiplet type has its own wafer flow.

Next, all the different wafers, each with a specific chiplet type, will follow the assembly and testing process before being assembled into a single package via heterogeneous integration. As an example, if a monolithic die is disaggregated into six chiplet types, each of the chiplet types will have its own wafer as well as fabrication, assembly and testing methods.

A significant benefit of this method is the ability to control the yield, test, validation, quality and reliability requirements of each chiplet. It also ensures that the specific chiplet type (part of an extensive complex chip) is correctly processed. The yield is not a concern, as each chiplet now has a modular and specific function that can be validated easily.

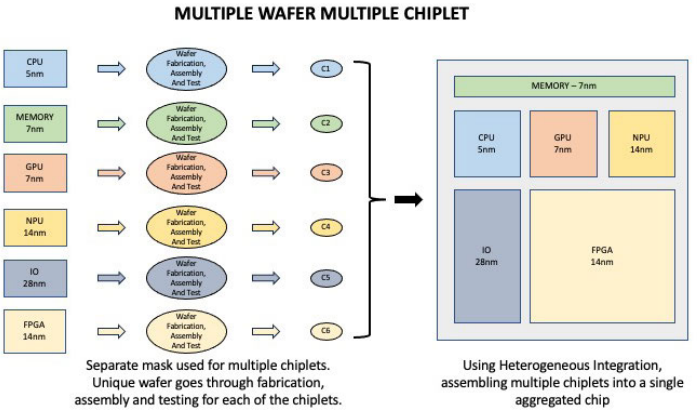


Producing a single chiplet type per wafer also ensures that all the chiplets on the wafer are subject to the same processing conditions, which can lead to more predictable yields. Moreover, it is easier to utilise and mix-match matured (above 40 nm) nodes with advanced (40 nm and below) nodes due to separate wafers. The single chiplet type per wafer method also enables a more controlled wafer flow that is easier to trace.

On the other hand, a significant drawback of the single chiplet type per wafer method is the number of wafers requiring supply chain management. There will be a need for as many human resources who can own and drive design to fabrication to validation to the production of each chiplet type. In addition, this method can increase the cost of productisation, as wafer fabrication, assembly, testing and other non-recurring expenses will add to the development cost.

Multiple chiplet types per wafer method

In the multiple chiplet types per wafer method, a wafer carries all the chiplet types that a monolithic die design is disaggregated into. Usually, a single mask is superimposed on the wafer, allowing for fabrication of the multiple chiplet types an area at a time. Once chiplets have been fabricated in one area, the mask is moved and the process repeated across the wafer until it is covered in chiplets.



A benefit of the multiple chiplet types per wafer method is that the multiple chiplet types are tested simultaneously on the fly using a single test program with various flows. Then, dicing and, later, assembly using heterogeneous integration allow for the creation of an aggregated chip. Another benefit is that the cost can be better controlled as the same human resources and tooling system can bring the chip to market. As an example, if a monolithic die is disaggregated into six chiplet types, each of the chiplet types is fabricated on the same wafer but in a different location.

A notable disadvantage of the method using multiple chiplet types per wafer is that certain chiplets, set to be assembled and tested using their specific flow, might be faulty due to fabrication errors. This results in an inconsistent number of functional chiplets available for creating an integrated chip at the heterogeneous level, potentially leading to waste if there is an imbalance in chiplet types on the wafer. Additionally, using a single mask to produce various chiplet types complicates the process, making it more susceptible to errors.

Way forward

To conclude, while the multiple chiplet types per wafer method is more flexible and lower in cost, it introduces complexities that manufacturers must navigate carefully. Conversely, the single chiplet type per wafer method can lead to better yield and provide more innovation opportunities.

As the industry has shifted towards modular and chiplet-based architectures, the focus has so far been on the multiple chiplet types per wafer method, including inventing new ways to efficiently test wafers with multiple chiplet types. Even Intel and AMD have so far focused on multiple chiplet types per wafer.

This does not mean that the single chiplet type per wafer method is not a sensible option. A significant advantage of this method is that more of the wafer area can be used because the chiplets are all the same size and fabricated directly next to one another. In the multiple chiplet types per wafer method, less of the wafer area can be used since the chiplet types vary in size and each type is fabricated in a different location.

Eventually, as more companies adopt the chiplet, they will have to weigh the pros and cons of single chiplet type per wafer and multiple chiplet types per wafer methods. The suitability of the method depends on the target application and system. ■

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