MORE-THAN-MOORE SoC: RISC-V, Chiplets, And Heterogeneous Integration

Ride the More-than-Moore wave! Established CPU and GPU giants are already on board, but it is the emerging startups leveraging RISC-V, chiplets, and heterogeneous integration that hold the key to a future of unparalleled AI-friendly SoC development

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More-than-Moore (MtM) is a concept and strategy in semiconductor design that extends beyond the traditional Moore's Law scaling of packing more transistors into a given silicon area (monolithic chips) to achieve performance gains. The MtM philosophy is fundamental as the physical and economic limits of traditional silicon scaling become apparent.

MtM aims to enable new applications by combining different technologies according to their functional needs rather than just focusing on making transistors smaller or faster. This strategy is increasingly seen as essential for the future of the semiconductor industry, enabling innovation in areas where silicon chips are running out of room to provide more performance gain.

The primary use of MtM is for system-on-a-chip (SoC) design and manufacturing, mainly because SoCs, sooner or later, will reach the reticle (photomask) limit. The reason is the theoretical EUV-based lithography reticle limit of 858mm^2, as the latest generation GPUs (following a monolithic approach) are already closer to 800mm^2.

It implies that there is little to no room to pack more transistors. Also, adopting the most advanced technology node to gain performance without increasing the area is slowly turning into a costly affair, with 3nm requiring more than $700 million to productise and 2nm needing more than $1 billion. Thus, there is a dire need to innovate SoC development.

MtM using RISC-V, chiplets, and heterogeneous integration

Out of all, the most promising combination of design and manufacturing approaches that will potentially speed up MtM adoption are RISC-V, chiplets, and heterogeneous integration.

The core reason is the three specific domains—design, fabrication, and packaging/testing—of SoC development, that each of these novel techniques is slowly and steadily revolutionising. Thus, enabling the fabless, Pure-Play fabs/IDMs, and OSATs with semiconductor technological solutions that can allow chip development without worrying about the reticle limit.

Design with RISC-V (pronounced RISC-five) in mind. RISC-V is an open standard in-

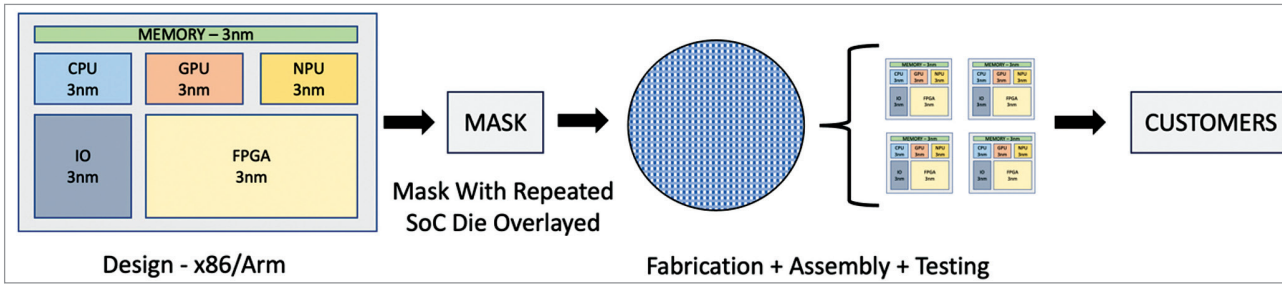

Fig. 1: SoC development—Moore way

struction set architecture (ISA) based on established reduced instruction selected computing (RISC) principles. Unlike proprietary ISAs, RISC-V is free to implement and is not subject to licensing fees, making it an attractive option for hardware developers looking to customise their processors for specific applications. It allows for a wide range of implementations, from tiny microcontrollers to high-performance servers, and supports a growing ecosystem of software and tools.

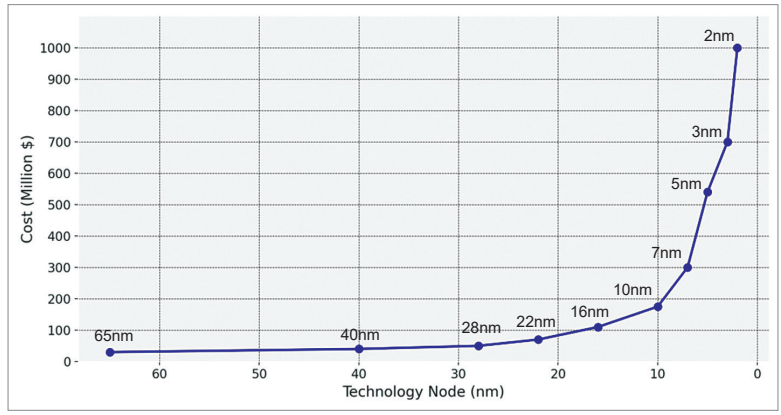

Fig. 2: SoC productisation cost based on technology node

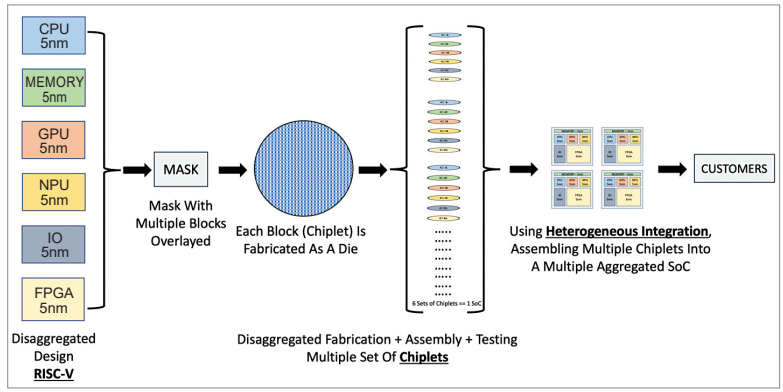

Fig. 3: SoC development—More than Moore way

Fabricate for chiplet flow. Chiplets are a novel approach to semiconductor design and manufacturing that involves creating minor, modular blocks of integrated circuits, each with a specific function, which get combined on a single package to form a complete system. It contrasts with the traditional monolithic approach, where all components are fabricated on a single silicon die. Chiplets enable greater flexibility and scalability, allowing chip architectures to meet the requirements of a specific application. Chiplets also allow for more efficient use of silicon area while enabling the use of different process nodes, thus lowering the cost of production.

Packaging/testing with heterogeneous approach. Heterogeneous integration refers to the advanced manufacturing technique in the semiconductor industry where diverse and separately manufactured components such as chiplets, memory, analog, digital, and photonic devices are integrated into a single system or package. This approach enables combining components that may be built using different materials and process technologies, optimising performance and functionality that cannot be achieved with homogeneous (monolithic) integration. Heterogeneous integration allows for greater design flexibility, improved performance through specialisation, and potential cost savings from yield enhancements and mature fabrication processes.

SoC development must always focus on utilising novel techniques that can defy the traditional way of SoC development to provide chip architects with more room to pack new features (like NPUs, different ASICs, eFPGAs, and so on).

Thus, MtM with RISC-V, chiplet, and heterogeneous integration can potentially revolutionise the SoC industry (mainly different types of XPUs), which is also at the core of the AI revolution. The more advanced the AI implementation is, the more influential the underlying SoC architecture should be. MtM's way of designing and developing SoC is the way to enable such high-performance architecture.

Future of More-than-Moore SoCs

The semiconductor industry (mainly the companies working on advanced SoCs) knows the benefits of the MtM solutions available today, but the rate of adoption could be much higher. Essentially, this is due to the ecosystem around RISC-V, chiplet, and heterogeneous integration, which is still under development. It will take about half a decade before the software-to-silicon ecosystem can enable SoC vendors to utilise these three breakthroughs efficiently.

Currently, the use of chiplet and heterogeneous integration is growing, with established CPU and GPU vendors leading the race. As more global emerging startups utilise the openness of RISC-V with the flexibility of chiplet and heterogeneous integration, the avenues to develop better AI-friendly SoCs will open, unlocking the market to speed up the adoption of such flow of SoC development.

Until then, the semiconductor industry is expected to follow Moore's way of designing and manufacturing SoCs with the More-than-Moore approach right behind it to enable more cost, node, and feature-friendly solutions for 1nm and beyond technology nodes. EFY

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