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Universal Chiplet Interconnect Express Will Speed Up Chiplet Adoption

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System-On-A-Chip (SoC) is the most complicated silicon chip that powers billions of computer systems, from smartphones to laptops to desktops to servers. SoCs are also responsible for running different applications, workloads, and operating systems. All of which are key to modern computing.

Historically, SoCs have always enjoyed Moore's law by leveraging the semiconductor manufacturing ability to integrate multi-millions of devices by utilizing the miniaturization of transistors. All while meeting the technical requirements, including maintaining the design and development cost.

However, as the semiconductor manufacturing of these SoCs has progressed towards advanced technology nodes (mainly 14nm and lower), the SoC design and manufacturing is slowly running out of room to pack more features (thus transistors) and raising challenges on managing power, performance, thermal and even cost profiles. It is a challenge equally applicable to other silicon chips that have started using advanced nodes.

To tackle complexities around the aggregated way of SoC design and manufacturing, the semiconductor industry is marching towards the More Than Moore era. The critical step in achieving such a goal is to leverage the chiplet way of SoC development.

Chiplets enable the development of SoC to be more disaggregated by splitting the blocks into multiple chiplets and then aggregating different chiplets at the package level. Doing is expected to provide performance that can cater to any futuristic compute and memory AI application, including providing more area to add features without compromising power, performance, and area (PPA) profile.

It is without any doubt that chiplet is going to open up avenues to leverage ultra- advanced technology nodes like 5nm and lower. It will also provide a roadmap to keep developing feature-rich AI-SoCs. AMD and Intel have already shown how promising chiplet is.

However, standardization will be essential to make the most of chiplet, which can also increase the chiplet adoption rate.

Reasons: Using multiple chiplet IPs from various vendors will be easier with a standard. Every IP vendor can adhere to the protocol (similar to how smartphones had different USBs and adopted USB-C) and will significantly speed up the open marketplace to mix and match IPs to create more innovative SoCs. There

will be no concerns about how to interface these chiplet IPs, and it will also help ensure that the manufacturing process, validation, and silicon bring-up are smoother than ever.

It is what Universal Chiplet Interconnect Express (UCIe) is focusing on achieving. UCIe is laying out specification details to enable Die-to-Die (chiplet-to-chiplet) interconnections and all critical specifications to speed up the chiplet adoption.

UCIe 1.0 focuses on the physical layer, protocol stack, software model, and compliance testing. All of which enable end users to mix and match chiplet components easily. Such a capability will allow multiple vendors to help drive the chiplet ecosystem and quickly choose IPs to develop more modular and customizable SoCs. UCIe 1.0 already has the backing of all the top semiconductor companies.

While interconnecting different chiplet using UCIe is step one towards mix and match approach. From a quality and reliability point of view, many critical technical details also need to be considered. To cover such a scenario, UCIe technical committee has started working towards UCIe 1.1. It focuses on reliability mechanisms to support broader usage models. And the most significant aspect it has added is to focus on automotive usage, which has stringent reliability and quality standards.

Vendors that will be UCIe compliant will be able to market their IPs swiftly, and having a common standard around chiplet also allows the semiconductor industry to ensure the design and manufacturing methods can speedily adopt chiplet flow, which is evident

from USB, Wi-Fi, Bluetooth, UWB, and several other standardized protocols that have enabled billions of silicon chip solutions only because of standardization.

A unified standard around chiplet also ensures that the assembly and testing part of the semiconductor product development can advance accordingly. Otherwise, without a chiplet standard, every die/chiplet will follow its flow, which is not a win-win situation.

As the semiconductor industry readies itself for the More Than Moore era, UCIe's standardization is certainly already playing a crucial role. As it evolves, it will likely bring the industry to advance silicon development without worrying about node-level constraints. Similar to what the Automotive Electronics Council (AEC) did for automotive semiconductors.

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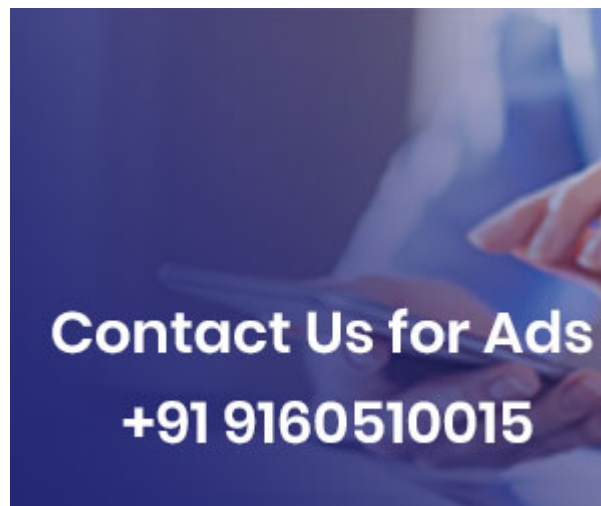
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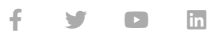
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