# Cost Challenges of Getting Advanced Semiconductor Products to Market

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Introducing a new leading-edge semiconductor product has become a daunting task. While transistor scaling continues, the economics of advanced semiconductor productization - spanning design, fabrication, packaging and testing - have increased the costs involved dramatically.

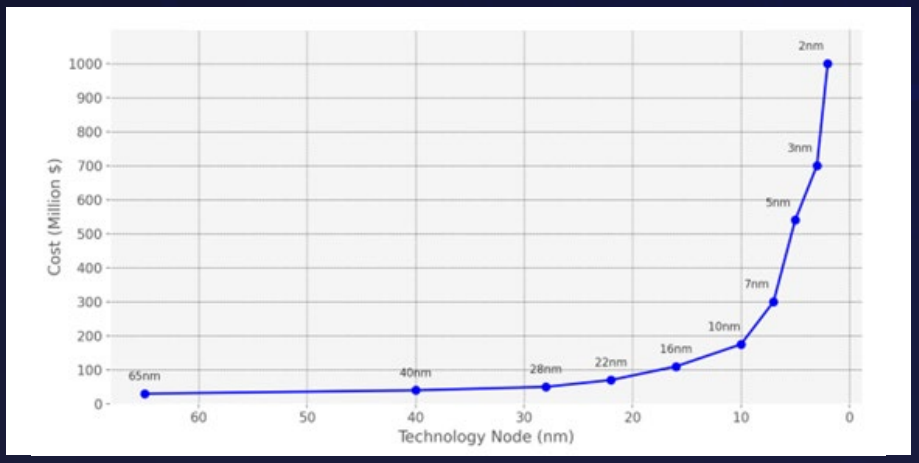


Figure 1: SoC productization cost based on technology node

Achieving high performance and efficiency at sub-7nm nodes requires massive capital investment, specialised engineering expertise, plus state-of-the-art manufacturing capabilities. All of this makes productization a risky endeavour, particularly for artificial intelligence (AI), high-performance computing (HPC) and automotive applications.

Historically, system-on-chip (SoC) productization costs only rose gradually from 65nm to 28nm. However, beyond 16nm, the cost curve turned exponential (see Figure 1). At 2nm, development and productization expenses are projected to exceed $1 billion, thereby restricting access to only the most well-funded semiconductor vendors and foundries.

Increasing chip design complexity, verification bottlenecks, plus adoption of extreme ultra-violet (EUV) lithography, have driven costs to record levels. Transition to chiplet and 3D packaging architectures further compounds the problem, requiring advanced interconnects, precision assembly and higher material overheads.

Ensuring yield, reliability and functional safety for AI accelerators, autonomous vehicle processors and data centre chips has also significantly increased testing and qualification expenses.

## Critical factors influencing productization costs

The rising expense of semiconductor productization is not just a byproduct of scaling, but a result of critical bottlenecks across design, manufacturing and validation. Each advancement in semiconductor technology introduces new challenges - requiring higher precision and more significant engineering effort, as well as specialised infrastructure - all of which contribute to an escalating financial burden.

One of the most pressing factors is the complexity of advanced node design. As transistors shrink, achieving power, performance and area (PPA) targets requires more extensive verification, longer simulation cycles and multi-billion transistor layouts - making design and validation exponentially more expensive. Additionally, reliance on 3rd-party IP and AI-driven optimisations has increased, leading to higher licensing fees and more significant design iteration costs. Table 1 summarises the key cost drivers and their respective impacts on advanced semiconductor productization. These factors illustrate how semiconductor

| Cost Factor | Reason for Increase | Impact on Productization |
|---|---|---|
| **Design and verification** | Growing transistor count, complex power/timing closure, increased EDA tool license and compute costs. | Higher engineering effort, longer development cycles and overall increase in design budgets. |
| **IP licensing** | Greater reliance on 3rd-party processor cores, memory controllers and connectivity solutions. | Licensing now represents over 50% of the total design cost, requiring companies to make trade-offs between custom design and external IP. |
| **Fabrication** | Advanced lithography, multi-patterning and lower process yields at smaller nodes. | Wafer costs exceeding $20K at 3nm, longer yield ramp-up and increased capital expenditure for manufacturing infrastructure. |
| **Mask sets** | Increased layer count, stricter patterning requirements, plus more complex design rule checks. | Limiting design iterations and increasing financial risk. |
| **Advanced packaging** | Transition from monolithic dies to chiplets, high-bandwidth memory (HBM) integration and 3D stacking. | Higher material and assembly costs, yield loss risks and the need for more advanced interconnect technologies. |
| **Testing and qualification** | AI, HPC and automotive chips require more extensive validation, burn-in testing and system-level characterisation. | Testing now accounts for 10% to 25% of total product costs, adding delays and slowing down overall time-to-market. |

Table 1: Cost drivers and the impact they have on productization

productization at advanced nodes has become a costly, multi-dimensional challenge - with rising expenses across design, fabrication, packaging and testing. As EDA complexity increases, yield optimisation becomes more complex and packaging transitions across to chiplet-based arrangements, the monetary outlay needed to bring a new chip to market will ramp-up further.

With mask set costs limiting design iterations, lower initial yields extending process refinements and rigorous testing requirements adding time-to-market delays, only companies with significant capital, manufacturing expertise and supply chain control can sustain cutting-edge development. Managing these factors will be crucial for companies looking to balance innovation, cost and scalability in next-generation semiconductor productization.

## Time-to-market & supply chain risks

As semiconductor productization costs rise, time-to-market delays and supply chain disruptions have become critical challenges. The increasing complexity of design, fabrication and validation at advanced nodes has extended development timelines, while geopolitical tensions and material shortages place further strain upon supply chains. Today, companies must navigate longer design cycles, limited foundry access and logistical uncertainties, all of which drive up costs.

At sub-7nm nodes, development timelines have stretched from 12 to 18 months to around 24 to 30 months - due to verification complexity, extended qualification cycles and lower initial yields. Testing alone accounts for over half of the development time, requiring extensive simulation and validation across billions of transistors. Missing a launch window can be costly, particularly in consumer, AI and industrial sectors - where even brief delays may mean that valuable market share is lost.

Foundry access has become a significant constraint, with only a few players capable of manufacturing at 5nm or below. High demand and limited capacity mean that only the largest semiconductor firms can secure wafer allocations, often requiring huge prepayments. Smaller firms face delays or must remain on older nodes, impacting their competitiveness. The recent global chip shortage exposed supply chain imbalances, with high-margin AI and consumer chips being prioritised over automotive and industrial devices.

Beyond fabrication, material shortages, export restrictions and logistics disruptions have added new risks. Critical components, such as EUV pellicles, high-purity neon gas and advanced packaging substrates, remain in short supply. The move to chiplet-based architectures has further complicated supply chains - requiring coordination across multiple foundries and outsourced semiconductor assembly/test (OSAT) providers. To mitigate these risks, semiconductor companies need to secure long-term capacity agreements, diversify suppliers and invest in localised manufacturing. Those that optimise design for manufacturability and yield early in development will gain a competitive edge in an increasingly constrained industry.

## Potential strategies to overcome rising productization costs

Managing the rising costs of semiconductor productization requires a strategic and adaptive approach across design, fabrication, packaging and supply chain management. As the complexity of advanced semiconductor manufacturing grows, cost-efficient methodologies and process optimisations are becoming critical to sustaining innovation while maintaining profitability.

To remain competitive, companies can focus on cost-efficient methodologies and process optimisations, including:

- Chiplet-based architectures and heterogeneous integration - Mixing different process nodes within a single package can reduce wafer costs and improve yield, but requires advancements in interconnect technology, packaging and system validation.
- Extending mature node utilisation - 28nm and 16nm remain viable for automotive, industrial and consumer applications, offering cost-effective alternatives without the high capital investment of sub-7nm nodes.
- AI-driven design automation - AI tools help optimise layouts, reduce design iterations and accelerate verification, lowering new product introduction (NPI) costs.
- Strengthening supply chain resilience - Securing foundry capacity, supplier diversification and localised manufacturing investments are crucial to mitigate risks from geopolitical uncertainties and material shortages.
- Optimising advanced packaging and OSAT coordination - As chiplets and 3D stacking grow in popularity, better supplier coordination and test methodologies will be key to controlling costs and improving yield.

## Conclusion

By implementing a combination of architectural shifts, design automation, supply chain resilience and manufacturing optimisations, semiconductor firms can better navigate the increasing costs of bringing advanced chips to market. These strategies will play a pivotal role in ensuring that technological progression remains economically viable, allowing companies to innovate while adapting to the realities of modern semiconductor economics. As the industry moves forward, the ability to streamline productization, manage costs effectively and optimise development cycles will define the leaders in the next era of semiconductor advancement.

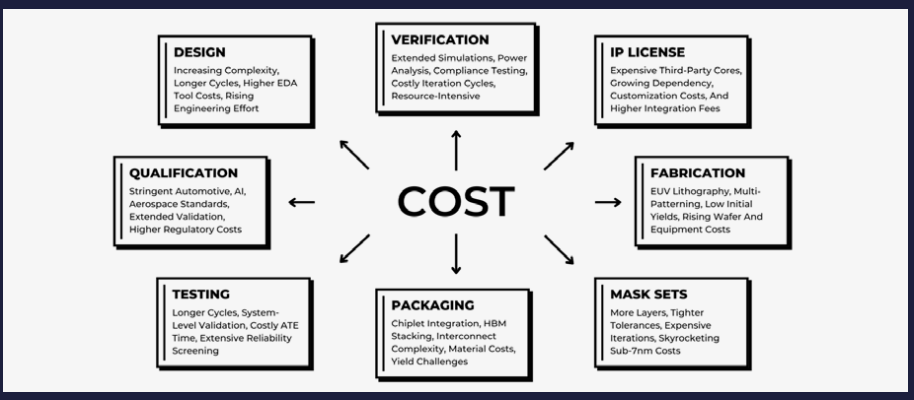


Figure 2: SoC productization cost based on technology node